REVISIONS			
LTR	**DESCRIPTION**	**DATE**	**APPROVED**
A	Correct the operating temperature range in section 1.3 and the pin out in section 1.2.2. - phn	12-09-20	Thomas M. Hess

Prepared in accordance with ASME Y14.24

Vendor item drawing

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REV STATUS OF PAGES	**REV**	A	A	A	A	A	A	A	A	A	A	A	A	A					
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13					

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.dscc.dla.mil**
Original date of drawing YY MM DD 12-04-09	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, LOW CAPACITANCE, LOW CHARGE INJECTION, ±15 V/+12 V *i*CMOS QUAD SPST SWITCHES, MONOLITHIC SILICON
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12617**
	REV **A**	**PAGE** 1 **OF** 13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low capacitance, low charge injection, ±15 V/+12 V *i*CMOS quad SPST switches microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12617	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADG1212-EP	Low capacitance, low charge injection, ±15 V/+12 V *i*CMOS quad SPST switches

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	16	JEDEC MO-153-AB	Lead thin Shrink Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

V_{DD} to V_{SS}	35 V
V_{DD} to GND	-0.3 V to +35 V
V_{SS} to GND	+0.3 V to -25 V
Analog inputs	V_{SS} - 0.3 V to V_{DD} + 0.3 V 2/ or 30 mA which ever occurs first
Digital inputs	GND - 0.3 V to V_{DD} + 0.3 V 2/ or 30 mA which ever occurs first
Peak current, S or D	100 mA (pulsed at 1 ms, 10% duty cycles max)
Continuous current per channel, S or D	25 mA
Operating temperature range	-55°C to +125°C
Storage temperature range	-65°C to 150°C
Junction temperature	150°C
16 lead TSSOP, θ_{JA} Thermal impedance (4 layer board)	112°C/W
Lead temperature, soldering	As per JEDEC J-STD 020

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95	–	Registered and Standard Outlines for Semiconductor Devices
J-STD-020	–	Joint IPC/JEDEC standard for moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices.

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Off leakage. The off leakage shall be as shown in figure 6.

3.5.7 On leakage. The on leakage shall be as shown in figure 7.

3.5.8 Off Isolation. The Off isolation shall be as shown in figure 8.

3.5.9 Channel-to-channel crosstalk. The channel-to-channel crosstalk shall be as shown in figure 9.

3.5.10 On Resistance. The on resistance shall be as shown in figure 10.

3.5.11 Bandwidth. The bandwidth shall be as shown in figure 11.

3.5.12 THD + Noise. The THD + Noise shall be as shown in figure 12.

3.5.13 Switching times. The switching times shall be as shown in figure 13.

3.5.14 Charge injection. The charge injection shall be as shown in figure 14.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2/	Limits						Unit
			25°C		-40°C to +85°C		-40°C to +125°C		
			Min	Max	Min	Max	Min	Max	
Analog switch									
Analog signal range							V_{DD} to V_{SS}		V
On Resistance	R_{ON}	V_S = ±10 V, I_S = -1 mA See Figure 10	120 TYP						Ω
		V_{DD} = +13.5 V, V_{SS} = -13.5 V		190		230		260	
On Resistance match between channel	ΔR_{ON}	V_S = ±10 V, I_S = -1 mA	2.5 TYP						
				6		10		11	
On Resistance flatness	$R_{FLAT(ON)}$	V_S = -5V/0 V/+V; I_S = -1 mA	20 TYP						
				57		72		79	
Leakage currents (V_{DD} = +16.5 V, V_{SS} = -16.5 V)									
Source off leakage	$I_{S(Off)}$	V_S = ±10 V, V_D = ∓10 V	±0.02 TYP						nA
		See Figure 6		±0.1		±0.6		±1	
Drain off leakage	$I_{D(Off)}$	V_S = ±10 V, V_D = ∓10 V	±0.02 TYP						
		See Figure 6		±0.1		±0.6		±1	
Channel on leakage	I_D, $I_{S\ (On)}$	V_S = V_D = ±10 V	±0.02 TYP						
		See Figure 7		±0.1		±0.6		±1	
Digital inputs									
Input high voltage	V_{INH}						2.0		V
Input low voltage	V_{INL}							0.8	
Input current	I_{INL} or I_{INH}		0.005 TYP					±0.1	µA
Digital input capacitance	C_{IN}		2.5 TYP						pF
Dynamic characteristics 3/									
	t_{ON}	R_L = 300 Ω, C_L = 35 pF,	65 TYP						ns
		V_S = 10 V; See Figure 13		80		95		110	
	t_{OFF}	R_L = 300 Ω, C_L = 35 pF,	80 TYP						
		V_S = 10 V; See Figure 13		100		115		135	
Charge injection		V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 14	-0.3 TYP						pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 8	80 TYP						dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 9	90 TYP						
Total harmonic distortion + Noise		R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz, See figure 12	0.15 TYP						%
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, See Figure 11	1000 TYP						MHz
	$C_{S(Off)}$	V_S = 0 V, f = 1 MHz		1.1					pF
	$C_{D(Off)}$			1.2					
	C_D, $C_{S\ (On)}$			3					
Power requirements (V_{DD} = +16.5 V, V_{SS} = -16.5 V)									
	I_{DD}	Digital inputs = 0 V or V_{DD}	0.001 TYP			1.0			µA
	I_{DD}	Digital inputs = 5 V	220 TYP			420			
	I_{SS}	Digital inputs = 0 V or V_{DD}	0.001 TYP			1.0			
	I_{SS}	Digital inputs = 5 V	0.001 TYP			1.0			

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 4/	Limits						Unit
			25°C		-40°C to +85°C		-40°C to +125°C		
			Min	Max	Min	Max	Min	Max	
Analog switch									
Analog signal range							0 V to V_{DD}		V
On Resistance	R_{ON}	V_S =0 V to10 V, I_S = -1 mA See Figure 10	300 TYP						Ω
		V_{DD} = 10.8 V, V_{SS} = 0 V		475		567		625	
On Resistance match between channel	ΔR_{ON}	V_S = 0 V to10 V, I_S = -1 mA	4.5 TYP						
				12		26		27	
On Resistance flatness	$R_{FLAT(ON)}$	V_S = -3V/6 V, 9 V/+V; I_S = -1 mA	60 TYP						
Leakage currents (V_{DD} = 13.2 V, V_{SS} = 0 V)									
Source off leakage	$I_{S(Off)}$	V_S = ±10 V, V_D = ∓10 V	±0.02 TYP						nA
		See Figure 6		±0.1		±0.6		±1	
Drain off leakage	$I_{D(Off)}$	V_S = ±10 V, V_D = ∓10 V	±0.02 TYP						
		See Figure 6		±0.1		±0.6		±1	
Channel on leakage	I_D, $I_{S\ (On)}$	V_S = V_D = ±10 V	±0.02 TYP						
		See Figure 7		±0.1		±0.6		±1	
Digital inputs									
Input high voltage	V_{INH}						2.0		V
Input low voltage	V_{INL}							0.8	
Input current	I_{INL} or I_{INH}		0.001 TYP					±0.1	µA
Digital input capacitance	C_{IN}		3 TYP						pF
Dynamic characteristics 3/									
	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V; See Figure 13	80 TYP						ns
				105		125		140	
	t_{OFF}	R_L = 300 Ω, C_L = 35 pF, V_S = 8 V; See Figure 13	90 TYP						
				115		140		165	
Charge injection		V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 14	0 TYP						pC
Off isolation		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 8	80 TYP						dB
Channel to channel crosstalk		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, See figure 9	90 TYP						
-3 dB bandwidth		R_L = 50 Ω, C_L = 5 pF, See Figure 11	900 TYP						MHz
	$C_{S(Off)}$	V_S = 0 V, f = 1 MHz		1.4					pF
	$C_{D(Off)}$			1.5					
	C_D, $C_{S\ (On)}$			3.9					
Power requirements (V_{DD} = +16.5 V, V_{SS} = -16.5 V)									
	I_{DD}	Digital inputs = 0 V or V_{DD}	0.001 TYP			1.0			µA
	I_{SS}	Digital inputs = 5 V	220 TYP			420			

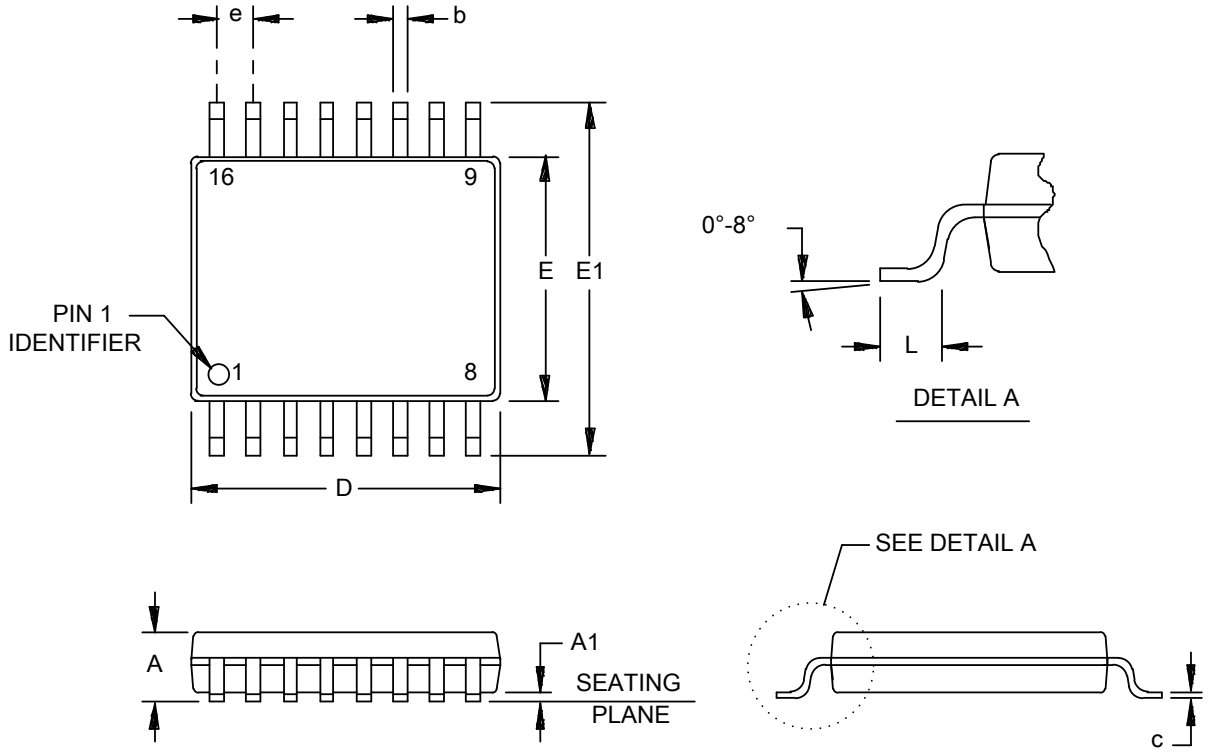
1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 15 V ±10%, V_{SS} = - 15 V ±10%, GND = 0 V, unless otherwise noted.

3/ Guaranteed by design, not subject to production test.

4/ V_{DD} = 12 V ±10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		1.20	E	4.30	4.50
A1	0.05	0.15	E1	6.40 BSC	
b	0.19	0.30	e	0.65 BSC	
c	0.09	0.20	L	0.45	0.75
D	4.90	5.10			

NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-15-AB3.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	IN1	9	IN3
2	D1	10	D3
3	S1	11	S3
4	V_{SS}	12	NC
5	GND	13	V_{DD}
6	S4	14	S2
7	D4	15	D2
8	IN4	16	IN2

NOTES:

1. NC = No Connect. Do not connect to this pin.

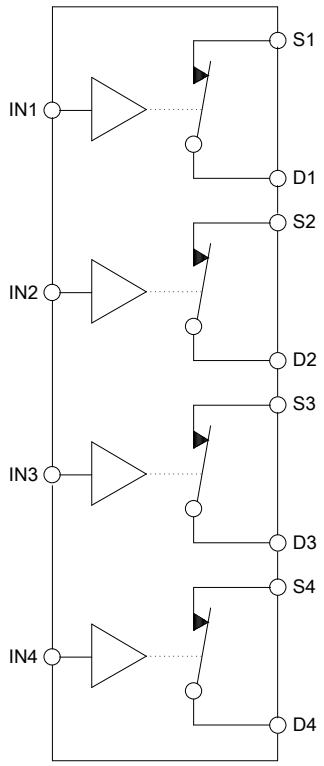
FIGURE 2. Terminal connections.

Case outline X		
Terminal		Description
Number	Mnemonic	
1	IN1	Logic control input.
2	D1	Drain terminal. This pin can be an input or output.
3	S1	Source terminal. This pin can be an input or output.
4	V_{SS}	Most negative power supply potential.
5	GND	Ground (0 V) reference.
6	S4	Source terminal. This pin can be an input or output.
7	D4	Drain terminal. This pin can be an input or output.
8	IN4	Logic control input.
9	IN3	Logic control input.
10	D3	Drain terminal. This pin can be an input or output.
11	S3	Source terminal. This pin can be an input or output.
12	NC	No connection.
13	V_{DD}	Most positive power supply potential.
14	S2	Source terminal. This pin can be an input or output.
15	D2	Drain terminal. This pin can be an input or output.
16	IN2	Logic control input.

FIGURE 3. Terminal function.

Input INx	Switch condition
1	On
0	Off

FIGURE 4. Truth table



NOTES:
1. Switches shown are for logic 1 input.

FIGURE 5. Functional block diagram.

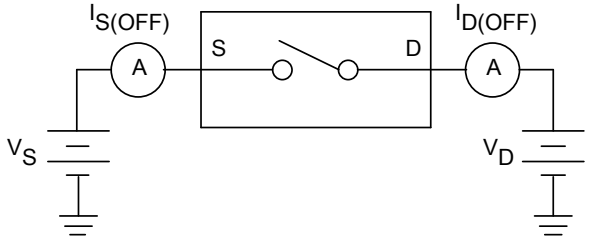


FIGURE 6. Off Leakage.

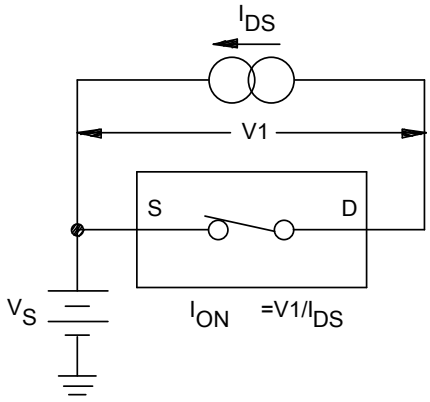
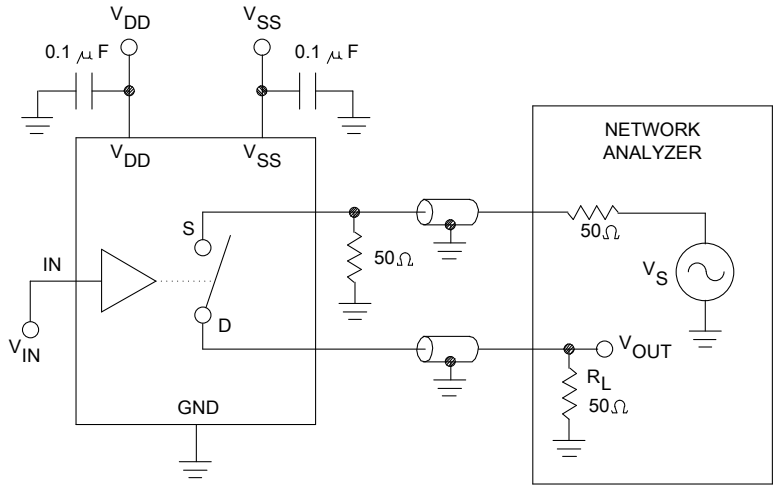
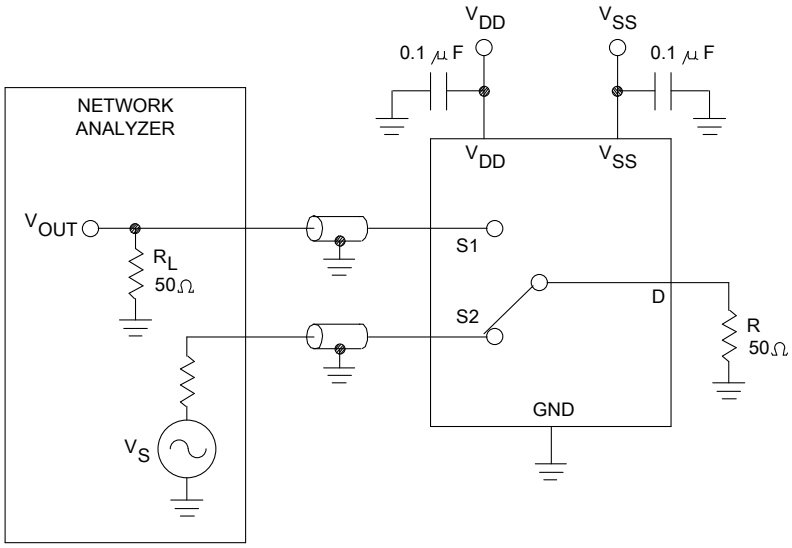


FIGURE 7. On Leakage



Off Isolation = 20 log $\frac{V_{OUT}}{V_S}$

FIGURE 8. Off isolation.



Channel-to-channel crosstalk = 20 log $\frac{V_{OUT}}{V_S}$

FIGURE 9. Channel-to-channel crosstalk.

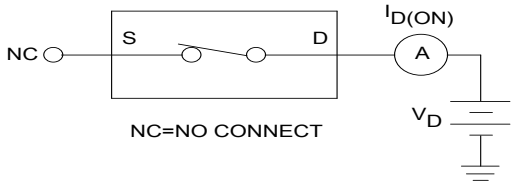
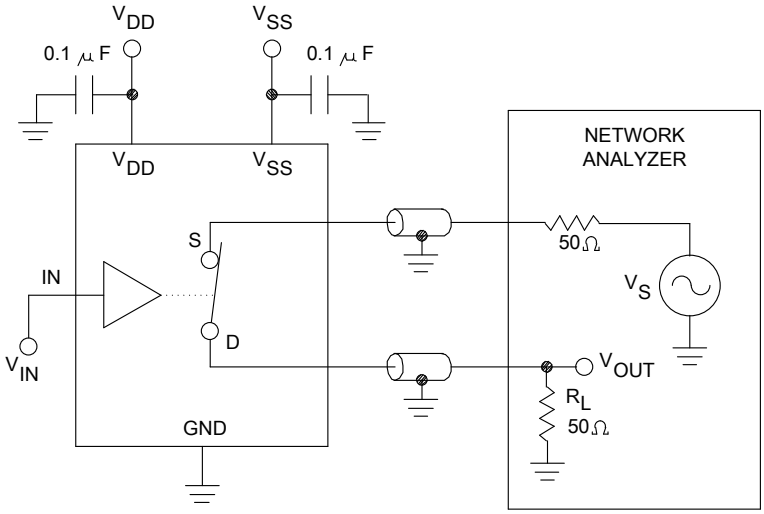


FIGURE 10. On resistance.



Insertion loss = 20 log $\frac{V_{OUT}\text{WITH Switch}}{V_{OUT}\text{WITOUT SWITCH}}$

FIGURE 11. Bandwidth

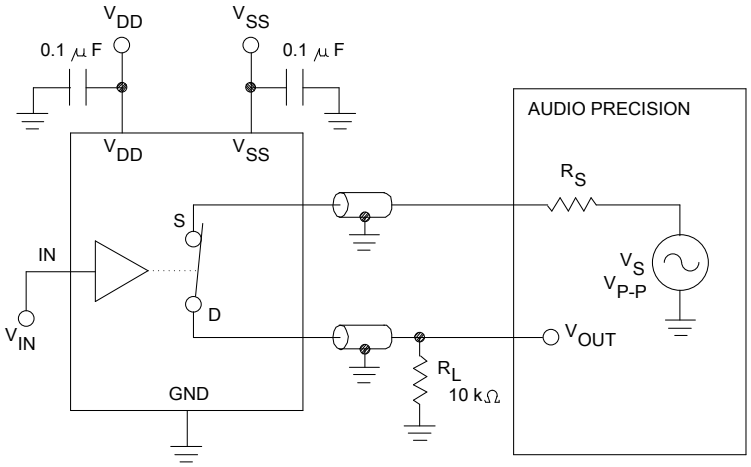


FIGURE 12. THD + Noise

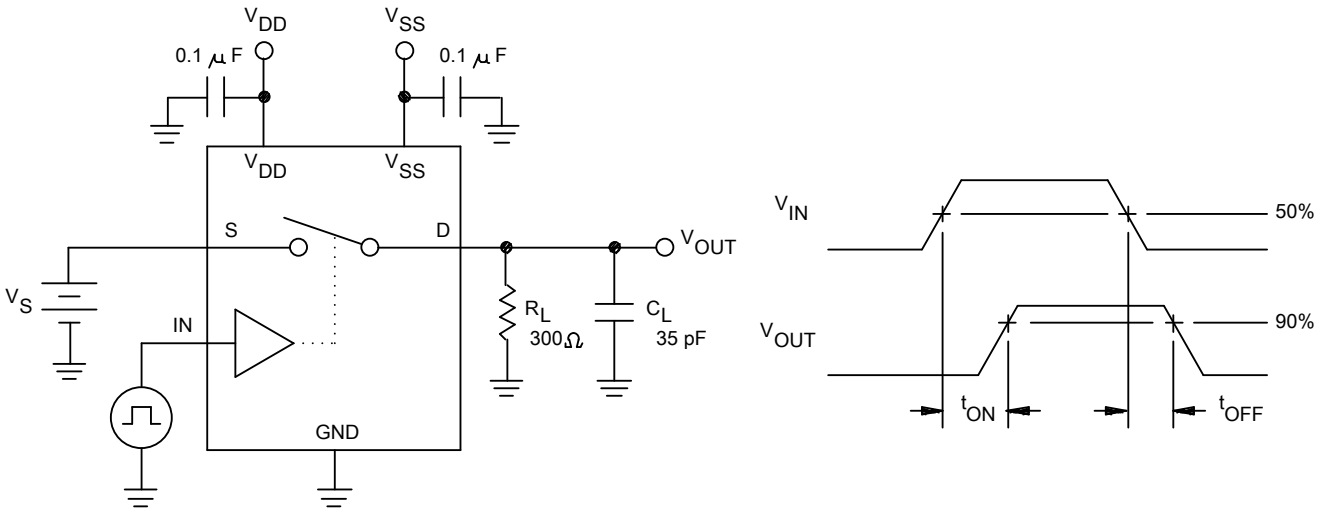


FIGURE 13. Switching times.

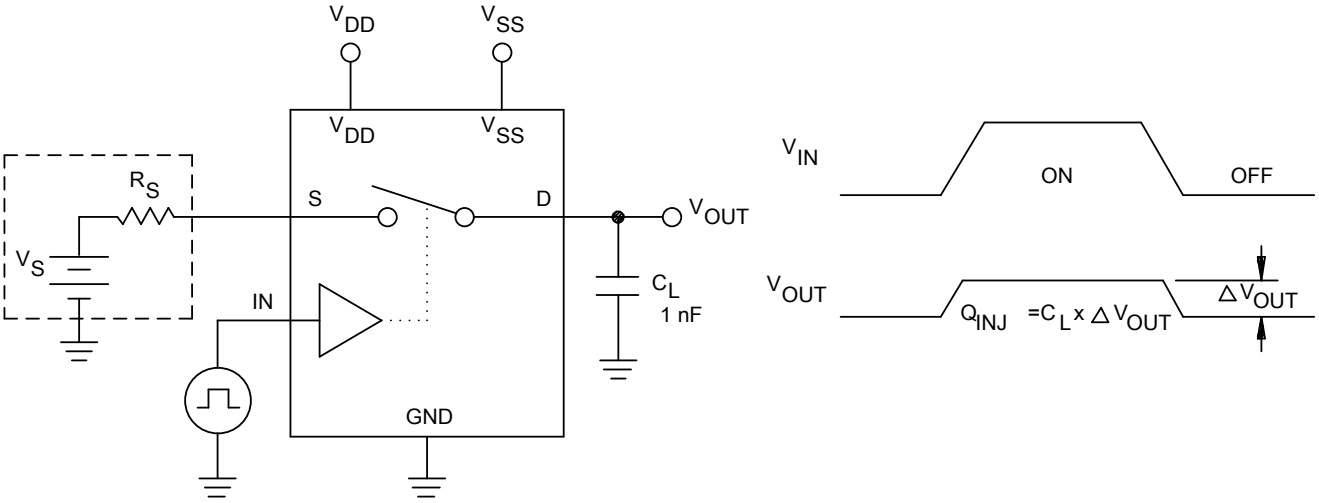


FIGURE 14. Charge injection.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/12617
		REV A	PAGE 12

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12617-01XB	24355	ADG1212SRU-EP-RL7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106